

Figure 1 (a)

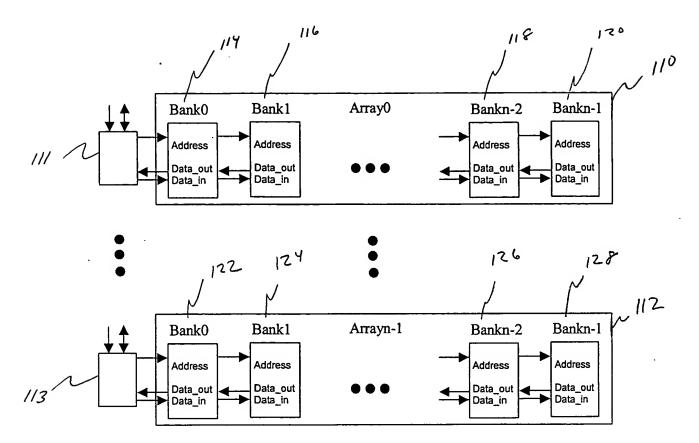


Figure 1(b). Systolic Memory Array

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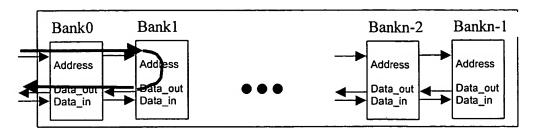


Figure 2(a) Read AdAddress/Data Movement

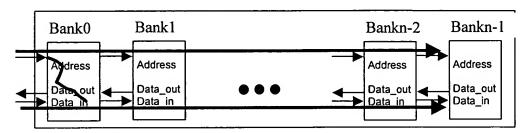
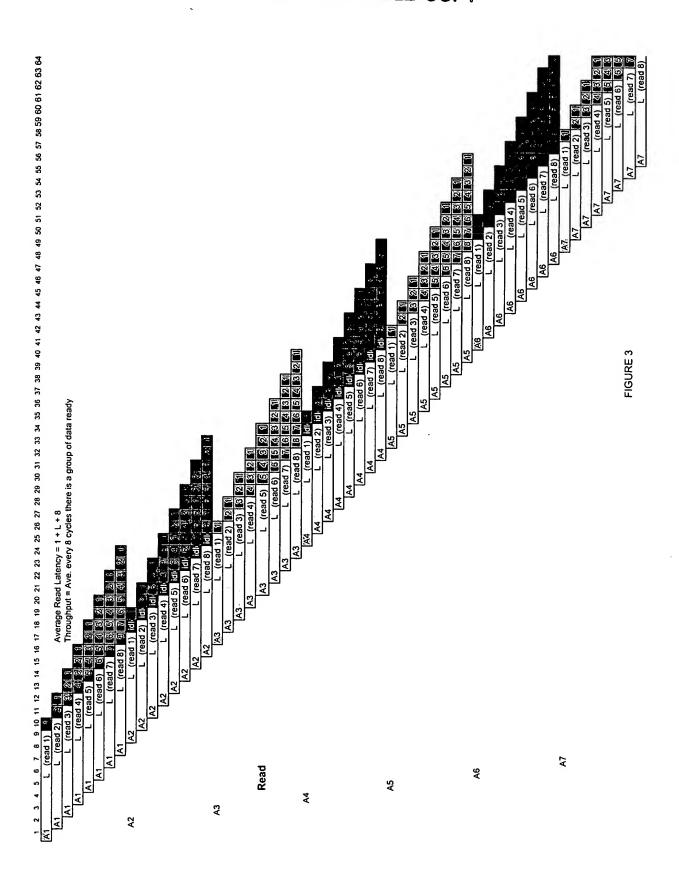
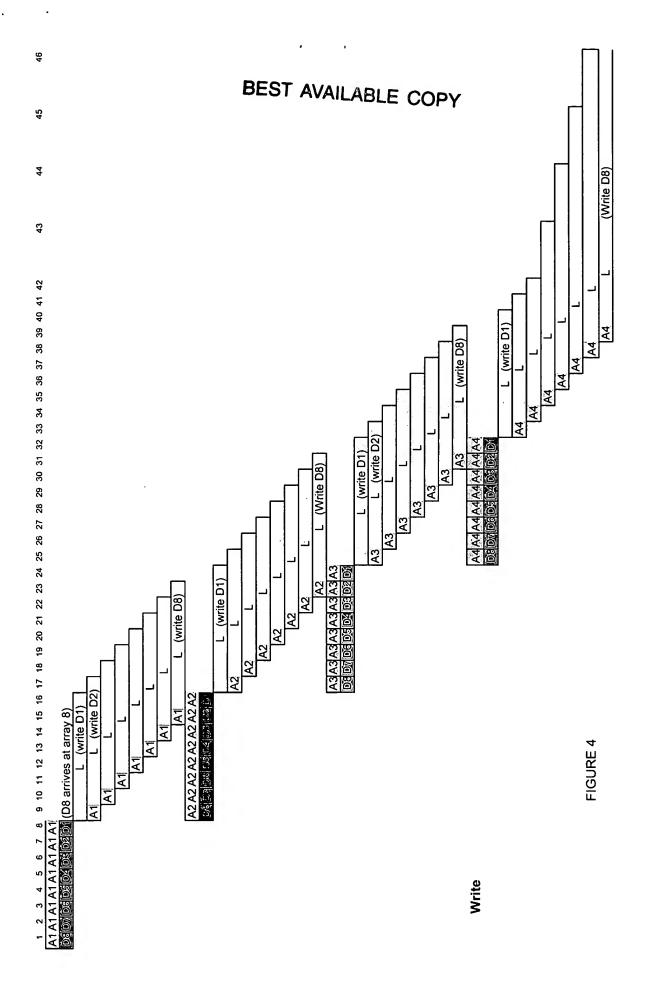


Figure 2(b) Write Address/Data Movement

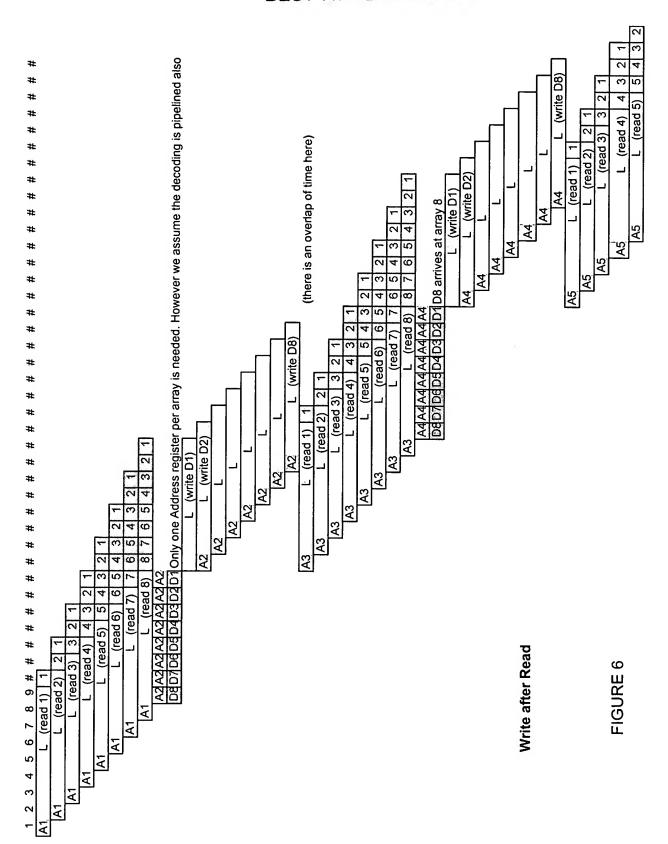
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BEST AVAILABLE COPY Only one Address register per array is needed. However we assume the decoding is pipelined also 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 We take advantage of the seperated read and write port to performance two operations (there is an 7 cycle overlap of read and write at each array) (read 8) 9 L (read 7) (write D8) (read 6) (read 5) If the read and write addresses the same we do bypass (read 4) (read 3) (read 2) (read 1) (wı (write D2) (write D1) D8D7D6D5D4D3D2D1 (D8 arrives at array 8) (read 7) (write D8) (read 6) (read 5) (read 4) (read 3) (read 2) (read 1) L (write D2) D월D계D역D4D3D2D1(D8 arrives at array 8) L (write D1) FIGURE 5 Read after Write 3 4 5 6 7 8 A1 A1 A1 A1 A1 A1 A1 A1

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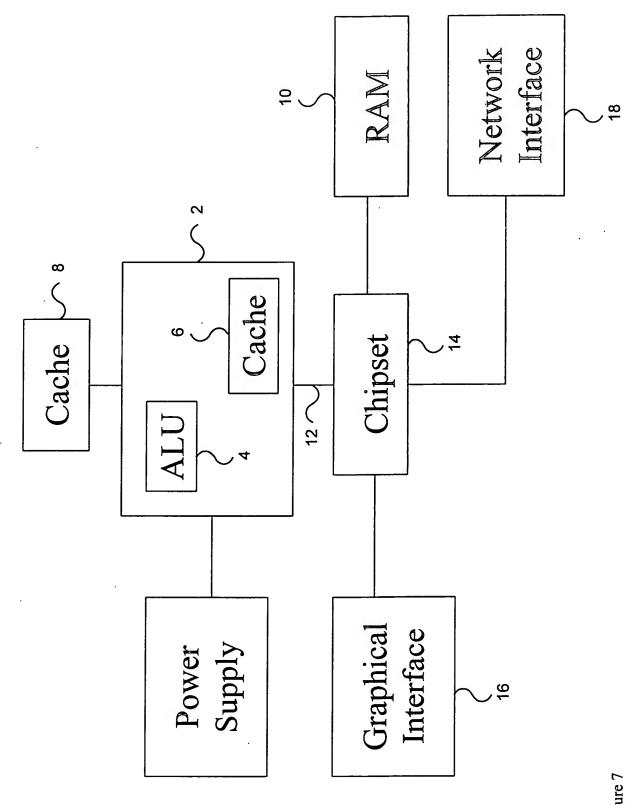


Figure 7